I CLAIM AS MY INVENTION:

1. A method for reducing printer errors while printing on a moving medium comprising the steps of:

transporting a print medium past a printhead and generating encoder pulses representing relative motion between said printhead and said print medium;

generating a counter count by incrementation and decrementation to identify an occurrence of a reduced time spacing between successive encoder pulses;

from a memory wherein binary pixel data are stored in a plurality of data strings, implementing a direct memory access in the time segment with DMA cycles for one of said data strings; and

implementing a print cycle for said one of said data strings to print data with said printhead, represented by said one of said data strings, on said print medium and, during said print cycle, implementing a further direct memory access in another time segment with DMA cycles from said memory for a next of said data strings to be printed and, following implementation of said further direct memory access for said next of said data strings and dependent on said time spacing for a plurality of successive encoder pulses, completely executing said print cycle as long as an average value of an encoder period of said plurality of successive encoder pulses does not downwardly transgress a predetermined duration of said print cycle, and aborting said print cycle if said counter count indicates said reduced time spacing.

2. A method as claimed in claim 1 comprising, dependent on the reduced time spacing from a number of encoder pulses, the spacing of the print cycles from one another is reduced until the following print cycle for printing out binary pixel data of a following data string follows immediately after a completely executed print cycle for printing out binary pixel data of a previous data string, whereby the reduction ensues to the extent that the encoder pulses lead the print cycles.

3. A method as claimed in claim 1 comprising, if said time spacing is not reduced, setting a duration for each print cycle to a time duration between two positive encoder pulse edges to space successive print cycles from each other and comprising identifying said reduced time spacing from said counter count by incrementing said counter count at each encoder pulse and decrementing said counter count at a beginning of each print cycle, and aborting a current print cycle if said counter count exceeds a predetermined reference value under the conduction that all direct memory access cycles for a next print cycle have ended.

4. A printing arrangement comprising:

a printhead;

a transport arrangement for transporting a print medium past said printhead;

an encoder that generates encoder pulses dependent on a relative movement between said print medium and said printhead;

a pixel memory containing pixel data representing pixels to be printed on said print medium by said printhead;

a print data controller for controlling transfer of said pixel data from said pixel memory to said printhead for printing in successive print cycles on said print medium by said printhead;

said print data controller comprising an evaluation unit and logic for reducing printer errors in printing by said printhead on said print medium, said logic being supplied with said encoder pulses and containing a resettable encoder clock counter having a count value that is incremented by respective leading edges of said encoder pulses and that is decremented with each start of each of said print cycles, said count value being supplied by said logic to said evaluation unit and said evaluation unit and said evaluation unit determining whether said count value exceeds a reference value, and causing a current print cycle to be aborted if said reference value is upwardly transgressed under the condition that all direct memory access cycles to said pixel memory for preparing a next print cycle have ended.

5. An arrangement as claimed in claim 4 wherein said print data controller comprises a DMA controller, an address generator, a printer controller and said address generator comprising said evaluation unit, and wherein said evaluation unit contains a register for storing said reference value and a comparator connected to said register and supplied with said count value from said logic for determining whether said reference value has been upwardly transgressed.

6. An arrangement as claimed in claim 4 wherein said resettable encoder clock counter has a counting range with an upper limit, and wherein said logic includes a first digital comparator that prevents decrementing of said count value if said count value reaches zero, and a second digital comparator that prevents incrementing of said count value if said count value reaches said upper limit and said encoder clock counter has an output connected to said evaluation unit for supplying said count value to said evaluation unit in said address generator.

7. An arrangement as claimed in claim 6 wherein said encoder clock counter comprises a decrementing input, an incrementing input and a reset input, and a plurality of outputs at which said count value is present as a multiple bit binary value, and wherein said outputs of said encoder clock counter are connected to first inputs of said first digital comparator and wherein said first digital comparator has a second input with a value of zero, and wherein said outputs of said encoder clock counter are supplied to first inputs of said second digital comparator, said second digital comparator having a second input connected to said register, and wherein said logic further comprises a first AND gate having a first input supplied with an output from said first digital comparator and a second input supplied with a decrement signal and an output connected to said decrementing input of said encoder clock counter, and a second AND gate having a first input connected to an output of said second digital comparator and a second input which receives said encoder pulses and an output connected to said incrementing input of said encoder clock counter.

8. An arrangement as claimed in claim 7 wherein said encoder clock counter is an n-bit counter, wherein n is said plurality of outputs.

9. An arrangement as claimed in claim 7 wherein said print data controller is supplied with said encoder pulses, a reset signal for said encoder clock counter, said decrement signal and said upper limit.

10. An arrangement as claimed in claim 4 wherein said print data controller is an application-specific integrated circuit.

11. An arrangement as claimed in claim 4 wherein said print data controller is formed by programmable logic.

12. An arrangement as claimed in claim 4 wherein said print data controller comprises a DMA controller, an address generator, a printer controller and said printer controller comprising said evaluation unit, and wherein said evaluation unit contains a register for storing said reference value and a comparator connected to said register and supplied with said count value from said logic for determining whether said reference value has been upwardly transgressed.